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A New VME Based High Voltage Power Supply for Large Experiments

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Disclaimer

A New VME Based High Voltage Power Supply for Large Experiments

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Abstract

A new VME based high voltage power supply has been developed for the DØ experiment at Fermilab. There are three types of supplies delivering up to ±5.6 kV at 1.0 mA or +2.0 kV at 3.0 mA with a set accuracy of 1.5 V and extremely low voltage ripples. Complete computer control has allowed many special features to be developed for the supply, including user-defined control and monitor groups, variable ramp rates, and advanced histogram and graphic functions.

I. INTRODUCTION

The computer controlled and monitored high voltage system designed and used at the DØ detector at Fermilab fulfills the experiment's needs for nearly 1,000 channels of compact, accurate supplies[1]. The system was designed around the VME-bus standard with up to 48 supplies per standard VME crate. Three types of supplies are in use (Figure 1). The first two are positive and negative polarity supplies capable of delivering between 10 V and 5.6 kV at 1.0 mA in steps of 1.36 V. The last is a positive polarity supply which delivers 10 V to 2.0 kV at 3.0 mA in voltage steps of 0.49 V. All three types are 100% drop-in compatible.

The setting error for all supplies is less than 1.5 V across the entire settable range. The setting is stable with acceptable voltage ripple levels of less than 100 mV rms at frequencies less than 1 kHz and less than 10 mV rms at higher frequencies. Computer controlled monitoring is achieved via 15 bit ADCs resulting in 170 mV and 32 nA least count sensitivity for voltage and current monitoring for the 5.6 kV supplies; the sensitivity for the 2 kV supplies is 62 mV and 100 nA.

The HV supplies were designed to be as simple as possible with complete computer control that incorporates many special features. For example, a common ramp rate can be defined in a group of up to four crates (192 supplies) and a maximum difference voltage between any two supplies in the group can be set. The computer monitors the voltage and current of the supply (keeping a running time history of current drawn) as well as the temperature of the module and the values of the low voltage supply voltages. The software can implement digital filters to improve the accuracy of the readback signal and also corrects for hardware inaccuracies in the supply. Variable ramp rates and user defined supply groups are other software features. Both PC and VAX software have been developed. Details of both systems are given in section IV.

II. MODULE DESCRIPTION

A. *Power Supply*

The power supply module consists of one control board and eight plug-in power supplies or channels (see Figure 2). Each channel has an SHV connector which protrudes through the front panel of the control board and a potentiometer which corrects for resistor tolerance (adjusted for ±5.6 kV supplies at 5500 V and for the +2 kV supplies at 2000 V). This calibration pot is not accessible during normal use.

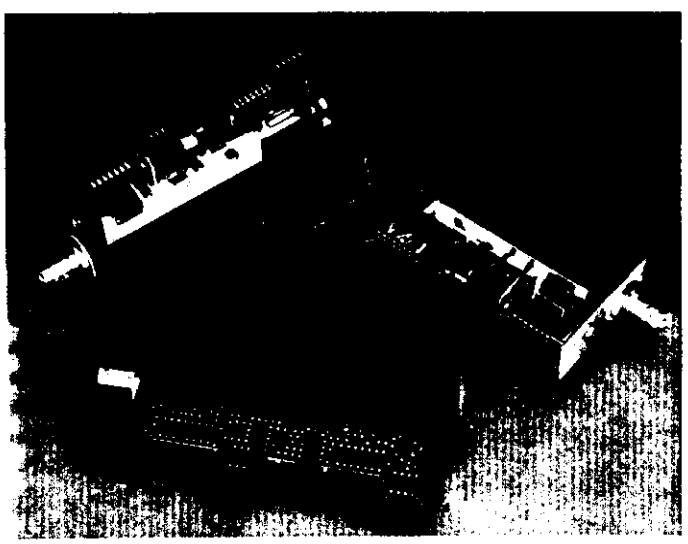

Figure 1: The three types of power supplies.

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Figure 2: A set of eight supplies on a control board.

Also located on the front panel are voltage limiting potentiometers used to set the maximum output voltage for each supply. A manual test point provides verification of this setting. Block diagrams of the control board and the supplies are given in Figures 3 and 4.

High voltage is generated within the supply by a pulse width modulator (PWM) and a voltage multiplier similar to a Cockroft-Walton generator. A fly-back transformer produces an AC signal which feeds the diode-capacitor chain of the voltage multiplier. The length of time that current is allowed to flow in the transformer is determined via a dual clock system, the command voltage, and the readback voltage. Clock B determines the start of current flow in the transformer. Clock A is used to generate a voltage ramp. The difference between the command and readback voltages produces an error signal that is compared with the ramp. When the ramp crosses the error signal, a CMOS switch opens and stops the current flow in the transformer. The third input to the AND gate is a power supply enable. There is also a redundant power supply disable signal (not shown) which forces the error signal above the ramp.

Current is measured by an operational amplifier in the ground return part of the transformer. The op amp forces the return current flowing back to the transformer to flow through the feedback resistor which then develops a voltage. This voltage is fed to the Over Current comparator and the ADC readbacks. The 10 Ω resistor is used to compensate for the 11 kΩ resistance in the HV output line as follows: When the supply is delivering a current of 1 mA (for example) there is an additional voltage drop of 11 V across the 11 kΩ resistor. When this is divided by 1120 it results in a 10 mV offset. If this were not corrected for, the voltage at 0 mA would differ from that at 1 mA by 11 V. One mA flowing through the 10 Ω resistor offsets the bottom of the divider resistor by 10 mV which compensates for the 11 kΩ resistor.

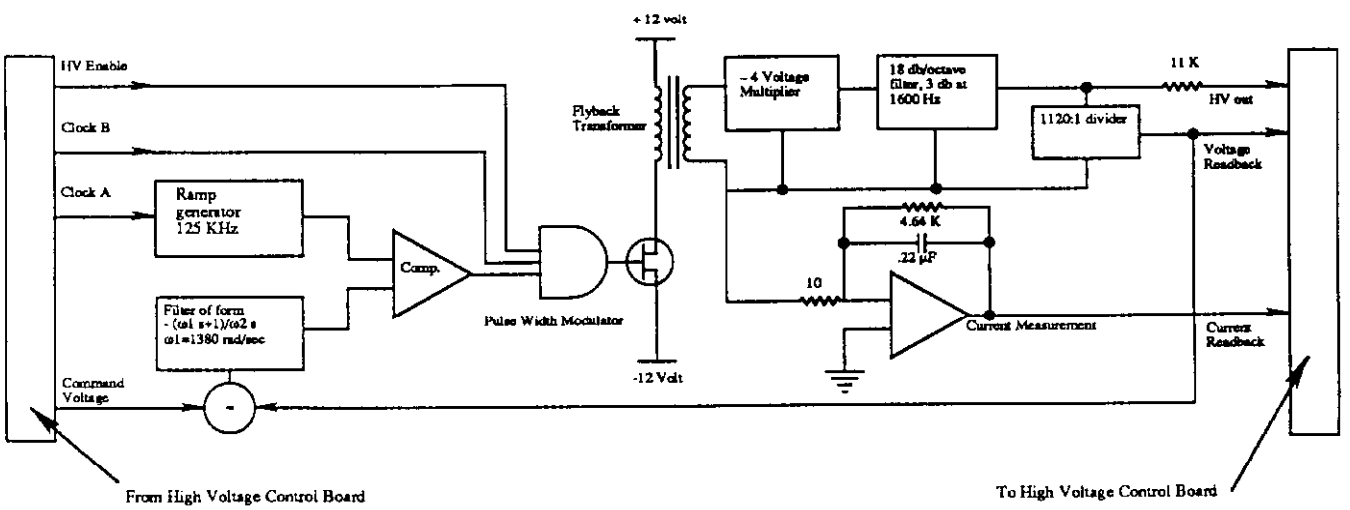


Figure 3: Block diagram of a high voltage power supply.

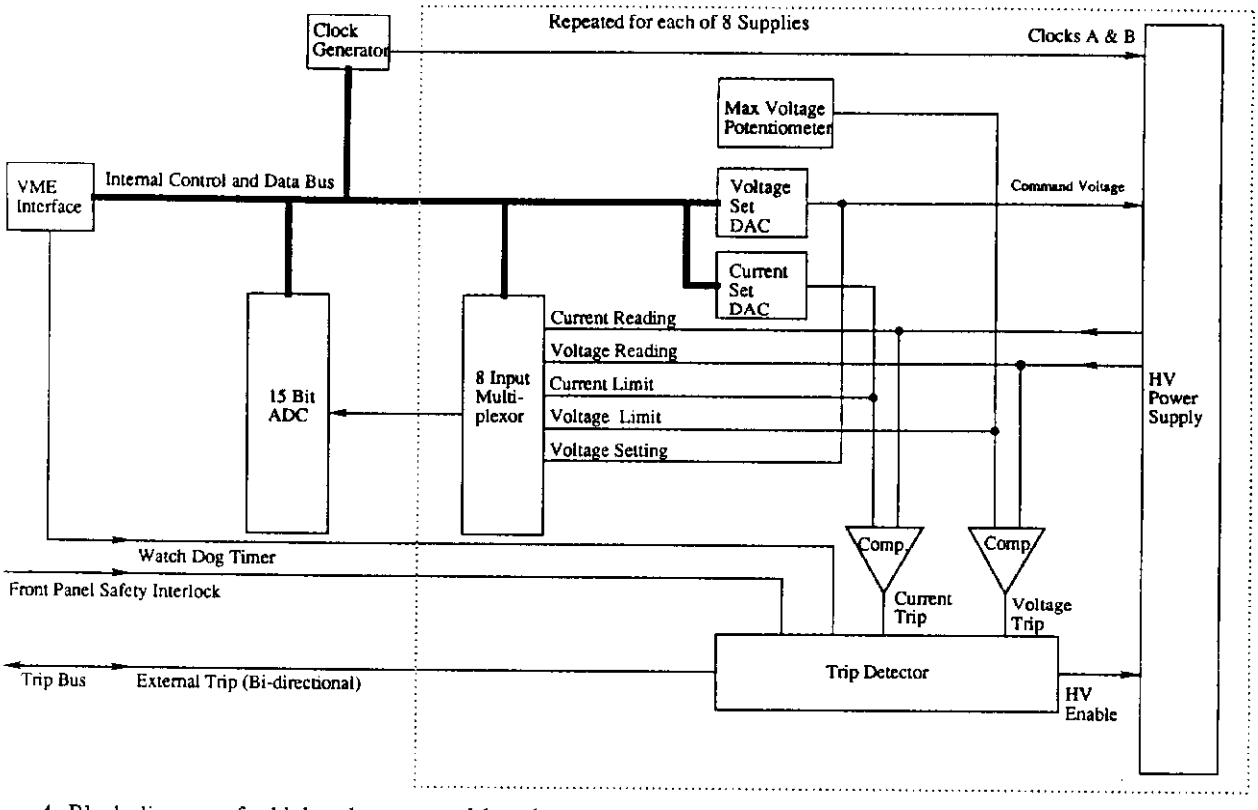


Figure 4: Block diagram of a high voltage control board.

B. Control Board

The control board supports the VME-bus interface, the digital control logic of the power supplies, and the ADC and DAC functions. Registers for control are located in the VME-bus address space on the control board. All high voltage control and status information is memory mapped into these registers. There are four registers per supply and four registers per module for the common ADC.

One 15-bit ADC digitizes analog signals for readback monitoring by the host computers, each reading taking a maximum of 50 μs. This ADC allows the user to monitor the voltage and current of the supplies, the values of the low voltage power supplies, the current and voltage limit settings, the command voltage, and the module temperature. A block diagram is shown in Figure 4.

The control board uses a standard VME backplane. However, a special (optional) J2 backplane was developed in order to prevent the switching noise from the fly-back transformer contaminating the ±12 V power. The backplane supplies ±12 V "dirty" power, ±12 V analog power, and +5 V power. The special J2 backplane uses different power supplies for the analog and "dirty" power. It should be used when low output ripple is required or when the current supplied by the J1 backplane is inadequate.

C. Safety

Each power supply trips on Over Current, Over Voltage, Watch-Dog Timer, External Interlock, and Module/Channel External Trip. These trips are hard-wired into the circuit so that the response to a trip is almost immediate. When the trip condition occurs and/or the supply is reset, the voltage control DAC is automatically reset to zero volts so that the supply is at zero when it is turned back on.

Over Current & Over Voltage Trips

Over Current and Over Voltage trips are handled by the control board. A dual comparator is used for each power supply. A supply is tripped off if the voltage or current exceeds the maximum values allowed by the user. The limits for these two trips are set via the software (current trip) and the front-panel trim pot (voltage trip). Both trips are "latched;" that is, the supply cannot be reenabled without user intervention.

Watch-Dog Timer Trip

The Watch-Dog Timer trip monitors the VME-bus activity. If there is no bus I/O after a certain length of time, the WDT trip is set. The length of time between bus I/O before a WDT trip condition occurs is adjustable from a fraction of a second to two minutes. This trip is also latched.

Interlock Trip

This latched trip is used to turn off the supplies in emergencies not related to the operation of the HV system (e.g. fire alarm at the detector, flammable gas leak). An interlock Lemo connector is located on the front panel of the control board. This connector must sink current at 5 V in order for the power supplies to be enabled. The signal can also come from the special J2 backplane.

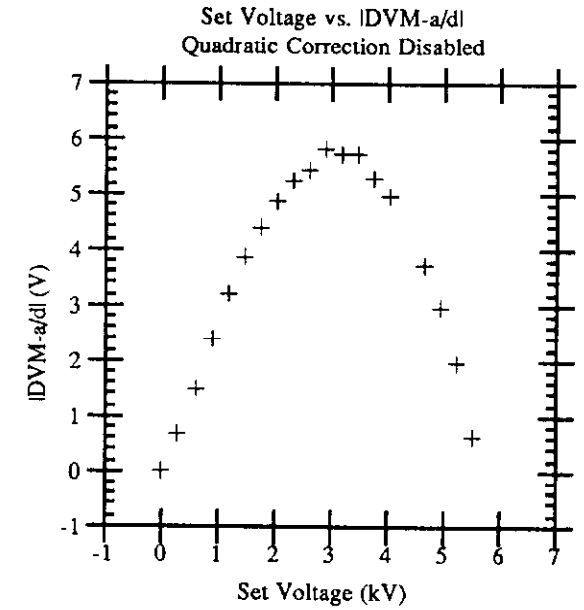
Module/Channel External Trips

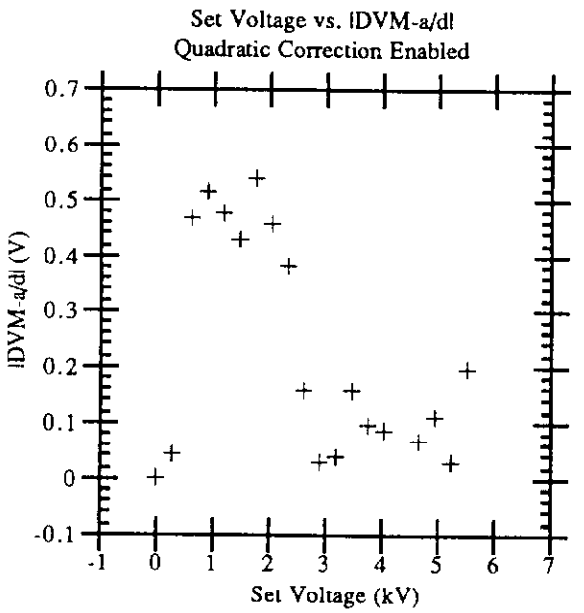
The J2 backplane developed for this system contains connections for the External Trip signals. The Module and Channel External trips are used to connect supplies or modules so that "trip groups" can be formed. If any supply in a trip group trips, all supplies in the group are disabled. This trip is

not latched. If the trip condition is removed, the supplies are reenabled at 0 V.

Software Trips

In addition to the hard-wire trips, the subordinate microprocessor located in the HV supply crate has software trips for Over Voltage and Over Current. This processor reads the voltages and currents of all supplies in a group over an "update cycle." For each channel it will check that the readback voltage is within the specified tolerance range and that the output current has not changed by more than a specified limit. If not, an Over Voltage or Over Current software trip is set. When this occurs, an additional malfunction notice indicates that the trip was software rather than hardware.





Figures 5 (top) and 6 (bottom): The difference between the DVM readback and the software readback for a typical supply with quadratic correction on and off.

D. Performance

A high precision, three terminal, high voltage divider-resistor was used to minimize temperature and aging effects. The resistance of this divider-resistor was found to vary parabolically with changing voltage[2] with a voltage coefficient of -0.7%/kV[3]. A Fluke precision DVM was used to measure the high voltage signal externally and coefficients for the quadratic nature of the computer voltage readback vs. DVM voltage readback were determined from a sample of approximately 40 supplies. The residual between the software readback reading and the DVM reading was then examined with the quadratic correction off (Figure 5) and on (Figure 6). An improvement by a factor of 10 was acheived using the quadratic fit.

The maximum difference (DVM reading minus a/d reading) was measured for approximately 80 supplies. The average difference was 0.9 ± .4 V; the maximum difference was less than 2.4 V (see Figure 7). The current readback was also tested for linearity and no correction was found necessary. Offsets for current readings were found to be less than 32 nA or one least count on the DAC.

The supplies are accurate and stable from 10 V to their maximum voltage. The maximum ripple is 100 mV rms but the typical ripple in a rack with 150 supplies is 50 mV peak to peak for frequencies less than 1 kHz and 10 mV for all higher frequencies (see Figure 8).

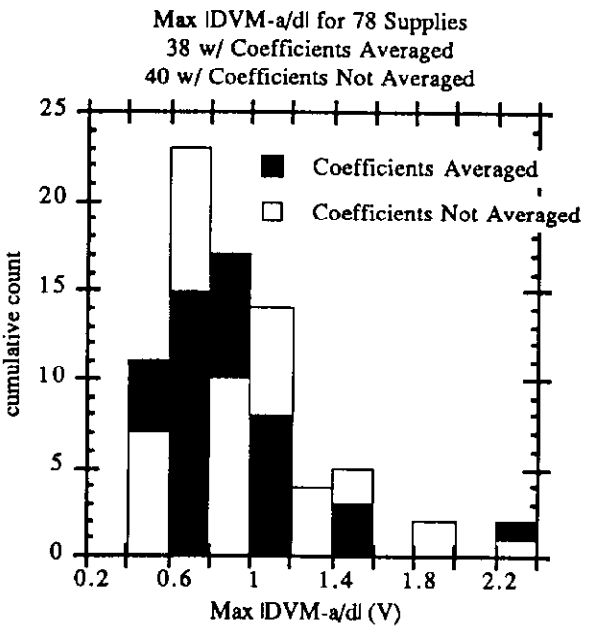


Figure 7: The maximum difference between the DVM reading and the software readback reading for 78 supplies, showing a mode of approximately 0.7 V--less than one least count on the DAC used in setting the voltage.

III. SYSTEM DESCRIPTION

The DØ system as designed has four HV crates and one master crate in each HV rack. Up to six modules fit in the crate, leaving room for a 68020 microprocessor and a slave

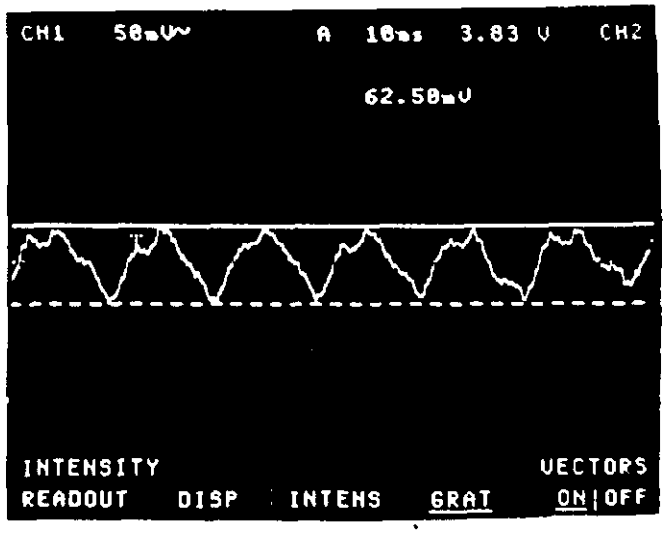


Figure 8: An oscilloscope trace of a typical noise ripple.

Vertical Interconnect that connects the HV crate to the DØ control system. The master crate contains the master Vertical Interconnect, VME-bus memory cards, PC to VME adaptor cards, a Token Ring card and a VME-bus 68020.

There are six racks reserved for supplies and two for HV computers and monitoring equipment at DØ. In addition to the four supply crates and the master crate, cooling fans, a networked 1553 rack monitor module, a rack monitor interface module, and an AC distribution box are mounted in the front of each HV rack. Each crate (including the master) has its own low voltage power supply mounted behind it. There are also two or three crates holding fanout or patch panels located in the back of the rack.

The supplies are used differently by each detector subgroup. For example, the Vertex drift chamber uses 168 supplies so that as little fanning out as possible is done. This allows the group to monitor current draw on wires on a sector by sector basis. It also avoids losing power on a large number of wires when one channel trips. Some other groups have extensive fanouts so that a few channels supply HV to their entire system. The Uranium/ Liquid Argon Calorimeters use a 1:16 fanout in some places to power their detector since there is less likelihood that a short will occur.

IV. SOFTWARE

The supplies are designed to be operated through the use of a host computer which has the ability to read and write to VME-bus memory. There are three different pieces of software running within a rack at any time: the master 68020 process, the subordinate 68020 process, and the Token Ring front-end process. The host computer (a VAX or PC) controls nearly all the operating aspects of the HV system through these processes. The host computers can also correct for various hardware inaccuracies. For example, it automatically accounts for any operational amplifier offsets in the supply's voltage readings by taking offset readings at 0 V. The host computer also corrects for non-linearities in the high voltage divider-resistor as described above. The software for the 68020, the PC and the VAX is described below.

A. 68020 Micro-Processor

The 68020 micro-processors are the means by which the supplies are controlled. The DØ HV racks have one subordinate processor for each power supply crate and a master processor and Token Ring front end processor for the master crate. The Token Ring front end process handles commands coming from the Token Ring network on behalf of the master.

The master accepts commands from the host computer via the Token Ring front end processor and coordinates the activities of all the subordinates in the rack. In addition, it keeps track of standard and affinity groups. A standard group is an arbitrary collection of channels defined by the host and known to the master; commands may be issued to affect all channels in this group. An affinity group has all of the properties of a standard group but in addition, it supports group trips. That is, if one channel in the group trips, then the master will force trips in all channels in that group. These groups are in addition to the hard-wired trip groups. The VAX computers access the high voltage system through the Token Ring local station card. The PCs use a PC-to-VME-bus interface to communicate with the master processor directly. While in operation, all the commands to the supplies are processed first by the master 68020 to ensure the integrity of the system.

The subordinate processor is responsible for the actual control of the power supplies and readback of all ADC signals. It also performs tasks such as checking transient current, checking voltage margin, updating the data structures, and updating the fast history, contained in the data pool. In addition, the subordinate executes the ramp step (specified by the host computer) used when ramping the supplies to a specified voltage.

The data pool allows external computers to read the last reading of a parameter from the dual port memory of the 68020 rather than setting an A-D channel number, waiting for the conversion, and then reading the value. The status of each supply is continually being read and stored into the pool by the subordinate processor. Specifically, the pool contains the last five minutes of history (the "fast history") of the values for voltage setting, current trip setting, voltage reading, current reading, current trip D/A readback, voltage A/D readback, voltage limit reading and voltage ramp rate.

In addition, the 68020s perform the update cycles. During an update cycle, the subordinate reads all channels, updates all states, and processes all commands from the master. A snapshot of the current state of every active channel is taken by the subordinate and this information is retained in a buffer to provide the fast history. The slow history is a variant of the fast history designed to show long-term trends (up to 24 hours) of the voltage and current readbacks only. It is updated approximately every five minutes by the master.

B. PC Software

There are two PC programs that control the HV supplies: HVD (High Voltage Display) and HV. HVD is the engineering version and contains approximately 16K lines of code. HV is the control version intended to be used with the

detector and is currently under development. Both were written and compiled in Turbo Pascal V6.0 and operate under MS-DOS 3.3.

HVD comes in three interface "flavors": two Bit3 flavors (polling and non-polling) and a Token Ring flavor. All three flavors use the same body of source code. The Bit3 flavors use a Bit3 board which interfaces a PC to a VME-bus board. The Token Ring flavor sends and receives messages to the HV over theToken Ring via a DØ control node. It has the advantage that it can be used wherever the Local Area Network exists.

HVD operates in three different modes: channel, module, or crate. For each mode, the on, off, reset, and ramp voltage or current features apply to either a single channel, a module of eight channels, or a complete crate, respectively. When ramping more than one channel to a specified voltage, the computer will stop if one supply trips for any reason.

HVD also has histogramming and graphing capabilities. It can plot the voltage setting, readback voltage, over-voltage trip setting, current reading, over-current trip setting, temperature, and the five voltages of the low voltage power supply (+5, +12, -12, +12 "dirty," and -12 "dirty"). The plots can be histograms or line plots over time. In addition, for the line plots, up to eight channels can be selected and plotted at once.

HV has more advanced group settings and plotting capabilities. It supports arbitrary groups across multiple slave crates. Its plotting capabilities include graphical meters which display the current and voltage readbacks and strip plots of voltage readback, current readback, or module temperature over time.

C. VAX Software

The VAX software operates over the Token Ring from any DØ VAX station. It is also still in the development stages. Some of its special features include the ability to support multiple users accessing the same HV unit and arbitrary group specifications for both monitor and control groups. The program keeps track of each user easily since all commands are sent to a central VAX first and then to the appropriate front-end process in one of the HV racks. This prevents two different users from taking control of a single HV channel or group.

The VAX program also downloads the voltage difference table to the 68020 processor. This table gives the voltage difference between any two channels. A maximum voltage difference can be specified between any two channels in a group such that all channels will be tripped off if that value is exceeded. This is especially important to some of the sub-detectors which are as sensitive to the voltage difference between wires as to the actual voltage on a wire.

Data can be displayed numerically and/or graphically according to the user. Other user-defined options include assigning aliases to the individual supplies and sorting the supplies into groups based on those aliases or any other criterion such as current or voltage reading or hardware database name.

The VAX program also logs the HV channel data. It keeps a fast history collected at 15 Hz and a slow history collected every five minutes. In addition to these, the VAX can periodically monitor and log the HV channels at user-defined frequencies. In case of a VAX or front-end crash, the program can recover to previous ownership and group structure status.

V. CONCLUSIONS

The new generation of large detectors make stringent demands on the quality and versatility of their high voltage supplies. Many detectors require turning several supplies off if one supply should trip. Using a large number of channels demands computer control so that groups of supplies can be ramped together and all supplies can be monitored continually. The rapid decline in the cost of commercial microprocessors led us to design a very simple supply and to use a processor to perform all the high level functions.

VI. REFERENCES

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[3] Military Standard 202F Method 309